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**Title of
Invention**

STRUCTURES AND METHODS FOR MANUFACTURING OF
DISLOCATION FREE STRESSED CHANNELS IN BULK SILICON AND SOI
CMOS DEVICES BY GATE STRESS ENGINEERING WITH SiGe AND/OR
Si:C

Application Number :

Date :

First Named Applicant: Hullong Zhu

Confirmation Number:

Attorney Docket Number: FIS920030375

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I, the undersigned, certify that I have viewed a display of document(s) being electronically submitted to the United States Patent and Trademark Office, using either the USPTO provided style sheet or software, and that this is the document(s) I intend for initiation or further prosecution of a patent application noted in the submission. This document(s) will become part of the official electronic record at the USPTO.

Submitted By:	Elec. Sign.	Sign. Capacity
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Documents being submitted:	Files
us-request	FIS920030375US1-usrequ.xml us-request.dtd us-request.xsl
us-assignment	FIS920030375US1-usassn.xml us-assignment.xsl us-assignment.dtd FIS920030375assign1.tif FIS920030375assign2.tif
us-fee-sheet	FIS920030375US1-usfees.xml us-fee-sheet.xsl us-fee-sheet.dtd FIS920030375dec1.tif FIS920030375dec2.tif
us-declaration	FIS920030375US1-trans.xml
us-declaration	us-application-body.xsl
application-body	application-body.dtd wipo.ent mathml2.dtd mathml2-qname-1.mod isoamsa.ent isoamsb.ent isoamsc.ent isoamsn.ent isoamso.ent isoamsr.ent isogr3.ent isomfrk.ent isomopf.ent isomscr.ent isotech.ent isobox.ent isocyr1.ent isocyr2.ent isodia.ent isolat1.ent isolat2.ent isonum.ent isopub.ent mmlextra.ent mmlalias.ent soextblx.dtd FIS920030375sheet1.tif FIS920030375sheet2.tif FIS920030375sheet3.tif FIS920030375sheet4.tif FIS920030375sheet5.tif FIS920030375sheet6.tif FIS920030375sheet7.tif FIS920030375sheet8.tif

Comments

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